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CHALLENGES IN INTEGRATING THE HIGH-K GATE DIELECTRIC FILM TO THE CONVENTIONAL CMOS PROCESS FLOW

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ABSTRACT

ZrO_2 and HfO_2 and their alloys with SiO_2 are currently among the leading high-k materials for replacing SiO_xN_y as the gate dielectric for the sub-100 nm technology nodes. International SEMATECH (ISMT) is currently investigating integration issues associated with this required change in materials. Our work has focused on the integration of ALCVD™ deposited ZrO_2 and HfO_2 with an industry standard conventional MOSFET process flow with poly-Si electrode. Since the impact of contamination by these new high-k materials introduced in a production fab has not yet been established, it becomes very critical to prevent cross-contamination through the process tools in the fab. A baseline study was completed within ISMT's fab and appropriate protocols for handling high-k materials have been established. The integrated high-k gate stack in a conventional transistor flow should not only meet all the performance requirements of scaled transistors, but the gate dielectric film should be able withstand high-temperature anneal steps. Reactions between ZrO_2 and Si have been observed at temperatures as low as 560°C (during the amorphous Si deposition process). Various wet chemistries were also evaluated for removing the high-k film inadvertently deposited on wafer backside, and it was found that ZrO_2 etches at extremely slow rates in the majority of the common wet etch chemistries available in a fab. A new hot HF based process was found to be successful in lowering Zr contamination on the wafer backside to as low as 1.8 E10 atoms/cm^2. The patterning of a high-k gate stack with poly-Si electrode is another area that required considerable focus. Various dry (plasma) etch and wet etch chemistries were evaluated for etching ZrO_2 using both blanket films as well as wafers with patterned poly-Si gate over the high-k films. On the full CMOS flow device wafers, most of these wet chemistries resulted in severe pitting in the ZrO_2 film remaining over the source/drain (S/D) areas, as well as in the Si substrate and the field oxide. A poly-Si gate over ZrO_2 gate dielectric film was successfully patterned using the standard poly-Si gate etch (Cl_2/HBr) for the main etch, followed by a combination of HF and H_2SO_4 clean for removing all of the ZrO_2 remaining over the S/D area. This allowed the fabrication of low-resistance contacts to transistor S/D areas, which ultimately resulted in demonstration of functional transistors with high-k gate dielectric films.

INTRODUCTION

Continued CMOS scaling beyond the 100 nm technology node may require replacing SiO_xN_y gate dielectrics with suitable high-k films in some high performance and low power applications. According to the International Technology Roadmap for Semiconductors (ITRS), the equivalent oxide thickness (EOT) would be 0.8 to 1.2 nm for the 70 nm generation [1]. The

gate leakage current for EOT = 1 nm with SiO_xN_y is ~ 100 amp/cm^2, which may be too high, especially for low power applications [2]. Currently the leading candidates for high-k gate dielectric films are HfO_2, ZrO_2, La_2O_3 and their alloys with SiO_2 and Al_2O_3 [3-8]. The thermal stability of the gate stack during CMOS processing (e.g. source / drain [S/D] activation anneal) is very critical for integration. Alloying MO_x with SiO_2 or Al_2O_3 ('Silicates' or 'Aluminates') improves the thermal stability at the expense of degradation in the dielectric constant [8-11].

For some of these films, EOT lower than 1 nm and very low gate leakage has already been demonstrated using MIS capacitors with metal electrodes as well as transistors with either metal or poly-Si gate electrode [3-7]. No high-k gate dielectric film has been demonstrated yet in a conventional CMOS transistor flow that meets all the roadmap requirements for 70 nm technology node. There is a big push from the industry to integrate the high-k gate dielectric into the industry standard CMOS process flow with the self-aligned poly-Si gate technology. The SiO_2 gate dielectric film along with poly-Si gate stack has been around for about 25 years, and has been demonstrated in a conventional transistor to as low as 30 nm gate length [12]. The primary reason for the success of the poly-Si gate is due to its high temperature thermal stability and the ability to dope it p- and n- type for CMOSFET. Replacing poly-Si gate with a metal electrode may require separate metals (different work functions) for PMOS and NMOS [13, 14]. This presents a serious integration challenge and will require extensive development. Novel transistor structures like vertical replacement gate (VRG) or FinFET that have previously been proposed would still require extensive development [15, 16]. Hence, there is a very strong interest in integrating the high-k films with the industry standard CMOS process flow with poly-Si gate electrode. However, there are many serious process challenges in integrating high-k films to industry standard CMOS process that need to be addressed.

HIGH-K GATE DIELECTRIC FILM INTEGRATION CHALLENGES

Some of the critical issues associated with integrating the high-k gate dielectric film to a conventional transistor are shown in Figure 1 [17, 18]. The high-k gate dielectric film should be able to withstand the processing steps including the S/D activation anneal step (e.g., RTA at 1000°C/10 sec for current technology) and still meet all the electrical specifications. The high-k film may react with the Si substrate and the electrode leading to the formation of interfacial layers.

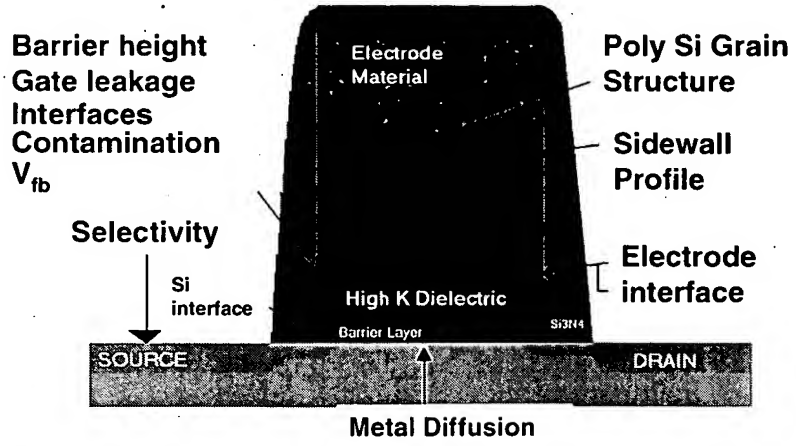

Figure 1 Schematic of the high-k gate stack showing some of the key integration issues

It is also likely that barrier layers may be intentionally deposited for reducing interfacial reactions and inter-diffusion. The high-k film and it's interfacial films would affect various device parameters like EOT, flat-band voltage (V_{fb}), barrier heights, gate leakage current, and channel mobility, and thus significantly affect the transistor behavior. Some of the metal oxides like Ta_2O_5, TiO_2, and BST are known to degrade when annealed at temperatures as low as 600°C [19]. The newer high-k materials including Al_2O_3, ZrO_2, HfO_2, and La_2O_3, as well as their alloys with SiO_2 have generated a lot of interest primarily due to their potential thermal stability in the presence of Si based on thermodynamic considerations [8-11].

From the process integration point of view, the presence of the high-k film and the interfacial layers in the place of the SiO_2 gate dielectric changes the etch requirements significantly. The gate dielectric film is typically used as an 'etch-stop' during the poly-Si etch process step. SiO_2 etch is very well characterized and films as thin as 1.5 nm are being currently used as an etch-stop layer for the poly-Si gate etch. On the other hand, there is very little data available on either dry or wet etching of ZrO_2, HfO_2 and other gate dielectric candidates. The high-k film left over the S/D area may affect the salicidation process and the contact resistance. High-k gate dielectric film, interfaces and the electrode present serious etch challenges. It is essential to have etch chemistries that can selectively etch the high-k film, as well as interfacial layers without etching either the poly-Si electrode or the shallow trench isolation (STI) SiO_2.

HIGH-K GATE STACK INTEGRATION DEVELOPMENT AT ISMT

The high-k film is not likely to be used as a gate dielectric until the year 2005 (70 nm technology node). However, it is still necessary to start focusing on the integration issues since most of the issues are likely to be very similar for the various metal oxide films even for the 70 nm technology. At International SEMATECH (ISMT), there has been a major focus on the integration of high-k materials into an industry standard 180 nm baseline CMOS-compatible flow using the currently available high-k films, even though these films may not be the ultimate film of choice for the industry by the 70 nm node. The initial focus was on ALCVD™ deposited ZrO_2 film. The choice of films has now been expanded to include ALCVD™ HfO_2 as well as MOCVD ZrO_2 and HfO_2. It is very important that contamination concerns are addressed before wafers with the high-k films can be introduced in a production fab and run on various process and analytical tools. The high-k integration development approach used at ISMT was to start the initial work with blanket high-k films on test wafers to narrow down the wet and dry etch chemistries as well as look at the thermal stability issues. The next stage was to move to the high-k gate stack short loop flows using a patterned poly-Si electrode over the high-k films to address the majority of integration issues. The final step was to complete the development using full flow CMOS-compatible device wafers.

HIGH-K CONTAMINATION ISSUES IN A FAB

The impact of contamination by high-k elements on transistor performance has not yet been completely characterized. This requires that any possible contamination due to introduction of wafers with high-k films in a production fab be carefully controlled. The cross contamination of the product wafers through the shared tools must be carefully monitored. This data can be

used to establish the necessary control limits for the tool. The impact of high-k contamination at various processing steps on the device performance needs to be established, and this data can then be used to establish contamination specification limits.

Since the high-k gate dielectric film is typically a metal-oxide film and is deposited in the front-end of the process flow, the contamination of front-end tools is more critical compared than the back-end tools. This is also the case since the back-end tools already have metal deposition steps as a part of multi-level inter-connect formation. Thus, the high-k contamination concerns are not very critical for processing the MIS capacitor or replacement gate transistor wafers, since these wafers are only processed through the back-end of the line tools after the high k film deposition. For the conventional transistor flow, the highest contamination risk tools are the ones used at gate stack etch, ash, post-ash clean, wet clean for resist removal, spacer etch and salicidation process steps. This is mainly because the high-k film is exposed on the wafer surface during these process steps.

High-k elements like Zr, Hf and La are not easily detectable using many existing TXRF models currently being used in most production fabs. New models of TXRF with Ag anodes are currently available that will be capable of detecting most of these elements. Since the TXRF model at ISMT (with W anode) was not capable of detecting some of the high-k elements, we had to use vapor phase decomposition inductively coupled mass spectroscopy (VPD-ICP-MS) for measuring the high-k contamination on test wafers.

The high-k film is typically deposited using a vapor phase deposition process. During the deposition step, some amount of film is inadvertently deposited on the wafer backside. It is very important to remove the high-k contamination from the wafer backside to prevent the transfer of the contamination during the wafer handling. This can be done by using a suitable wet chemistry on a wet spin processor tool [20]. Various wet chemistries were evaluated, and ZrO_2 was found to etch in HF. Table 1 shows the Zr level on the wafer backside immediately after a 5 nm high-k film deposition (on the wafer frontside) was as high as 2.3E14 /cm^2. When this wafer is capped with amorphous Si deposited in a furnace, some amount of Zr is still detectable on the wafer backside. This makes it necessary to ensure that a backside wafer clean is performed on wafers immediately after the high-k film deposition. Zr contamination dropped by 300x by using dilute

Test	Recipe Details	Zr Conc. By VPD (cm^{-2})
VPD Detection Limit		5 E07
Blank Si test wafer		6.5 E07
ZrO_2 wafer backside		2.3 E14
ZrO_2 wafer with poly cap		3.4 E10
Dilute HF backside clean	10:1 HF, 25C, 30 sec	1.7 E14
Dilute HF backside clean	10:1 HF, 25C, 120 sec	8.2 E13
Dilute HF backside clean	10:1 HF, 25C, 300 sec	6.6 E11
49% Hot HF backside clean	49% HF, 50C, 120 sec	1.9 E09
49% Hot HF/HNO_3 backside clean	Sequence in 49% HF and HNO_3	1.8 E10

Table 1 Zr concentration on the wafer backside as measured by VPD-ICP-MS before and after various HF based backside cleans steps.

HF for 5 minutes. However, by using hot concentrated HF, Zr concentration on wafer backside dropped even lower and below the fab baseline levels.

It is necessary to establish a baseline contamination level on the tools before introducing wafers with high-k into fab. The base-line concentration levels of all the high-k elements of interest were collected on 36 tools within the ISMT fab using VPD-ICP-MS with the majority of the tools in low E9 atoms/cm^2. Once this stage was completed, full flow transistor wafers with the high-k gate dielectric films were gradually introduced through the process tools starting in the middle of the year 2000. Contamination on each of the critical tools has been regularly monitored and a considerable database of contamination data has now been accumulated. So far, no high-k contamination of any tool has been detected due to the mechanical handling of the high-k wafers on a variety of process and analytical tools. Also on a multi-chamber cluster tool that has only one chamber for depositing MOCVD high-k films, it has been observed that no contamination from the high-k chamber was being transferred onto the robot blade or to the transfer chamber. There has also been no detectable tool contamination during high temperature rapid thermal anneal (RTA) of wafers with exposed high-k films. The tool used for etching the gate electrode by reactive ion etch (RIE), which has plasma directly exposed to high-k film, showed greater than E12 atoms/cm^2 levels of Zr contamination. We were successful in lowering the level of contamination on this tool considerably, but could not lower it enough to its original baseline contamination level. It would be necessary to use a dedicated high-k tool at the gate electrode etch process step. Currently at ISMT we continue to build our contamination database on the key process tools and are also continuing to work on doing a detailed analysis on the impact of the high-k contamination on the baseline transistor performance.

HIGH-K ETCH DEVELOPMENT USING BLANKET HIGH-K FILMS

The primary use of the high-k wet etch, in addition to the backside wafer clean as discussed in the previous section, is to remove the remaining film over the S/D areas after the gate electrode etch. The etch rates for ZrO_2 were evaluated by etching blanket ZrO_2 films on Si test wafers in a wet bench, wet spin etcher, or a lab beaker in various available wet chemistries. Etch rates presented in Table 2 were calculated by measuring the ZrO_2 film thickness before and after etch.

Etch Chemistry	Tool type	Etch Rate [Å/min]
SC1 (180s) + SC2 (60s)	Wet Bench	negligible
4:1 SPM for 120s	Wet Bench	negligible
10:1 HF for 78s	Wet Bench	4.39
10:1 HF for 60s	Spin Process	16.71
70% HNO_3 for 60s	Spin Process	2.95
4:1 SPM + 200A HF Etch + RCA	Wet Bench	negligible
182C H_3PO_4 (13 minutes)	Wet Bench	11.5
20% KOH for 180s	Wet Bench	negligible
HF/HCL (7:1) for 78s	Wet Bench	11.85
Hot Sulphuric (96% in 150C)	Wet Bench	0.583

Table 2 ZrO_2 wet etch rate in different etchants using either a wet bench or a spin process ZrO_2 is etch resistant to most common fab etch chemistries and etches very slowly in hot H_3PO_4 and HF only.

The other option is to use a reactive ion etch (RIE) to either thin down or completely remove the high-k film by a plasma etch process. However, the plasma etch could result in damage to the underlying Si substrate. From the process perspective, the high-k gate dielectric could be thinned down immediately after the electrode etch. To test this, blanket ZrO_2 films were etched on the poly-Si etch tool using the main electrode etch, the over etch step, and a CF_4 etch. Table 3 indicates the etch rates that were obtained. The etch rate was very low for both the poly-Si main etch and the over-etch chemistries, but much higher for the CF_4 etch. Such a chemistry may prove useful in the dry etch removal of high-k films over the S/D areas.

Dry Etch Process Step	ZrO_2 Etch Rate [Å/min]
Cl_2/HBr (Poly Si main etch)	10
HBr/O_2 (Overetch)	0
CF_4 (For high-k thinning)	54

Table 3 Blanket ZrO_2 film etch rates during various poly-Si etch tool

ETCHING THE PATTERNED HIGH-K GATE STACK

The next stage of development was to etch patterned wafers using gate short loop flows. The process steps used on this flow were as follows: deposit ZrO_2 on the test wafers → amorphous Si deposition (560°C) → Ion Implantation → Poly-Si activation anneal (RTA 1000°C/10 sec) → Litho → Poly-Si etch → Ash and clean. Figure 2 shows the SEM of the patterned poly-Si electrode after gate etch as well as followed by the ash process step.

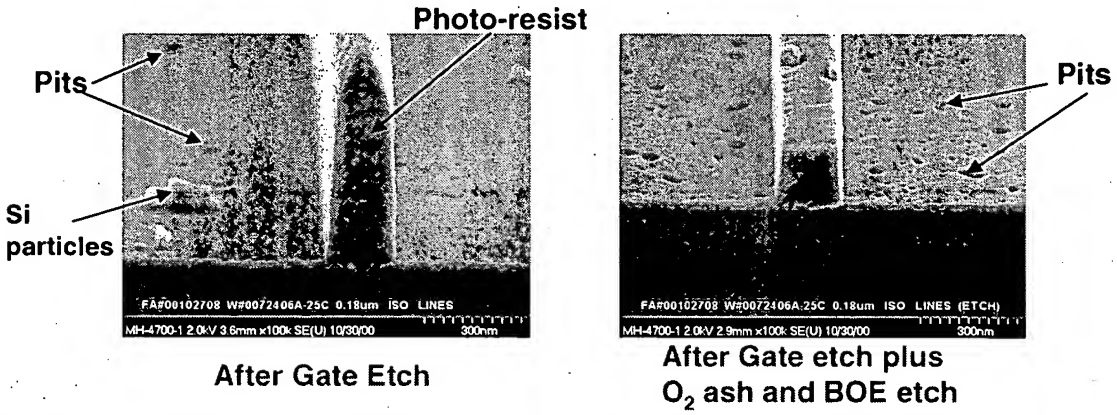

Figure 2 SEM of poly-Si/ZrO_2 gate stack after gate etch and followed by O_2 ash showing pitting in the ZrO_2 remaining over the S/D areas

Small pits were observed in the ZrO_2 film remaining over the S/D areas after the gate etch process step. The density of the pits increased significantly after the ash and the BOE

steps. The same test was also performed after removing the poly-Si activation anneal step from the process flow. Pitting in the ZrO_2 film was still observed, but the density of the pits was significantly lower. The presence of the pits in the short loops was not seen during any of the wet etch tests that were done on blanket, unpatterned ZrO_2. Thus, the integrated effects of the process steps can produce very different results due to the changes in the high-k films associated with different thermal, chemical, gas, plasma or material exposure during the integrated device fabrication steps. Detailed tests were performed to understand the origin of the pits in the ZrO_2 gate dielectric short loops with the Si gate electrode. Wafers with blanket ZrO_2 films were subjected to each of the process steps and were examined for pitting. It was observed that none of the steps associated with electrode etch by themselves caused pitting. Also, just subjecting the ZrO_2 film to the same thermal anneal (560°C, 2 hrs) as seen during amorphous Si deposition in a furnace did not result in any pitting. However, after the ZrO_2 was covered with an amorphous Si and after the Si was etched away using wet chemistry, pitting was observed. This indicates that there is some reaction in isolated areas between the ZrO_2 and the Si during the amorphous Si deposition process. It is likely that the reaction product is etched away very selectively compared to the bulk ZrO_2 films resulting in the formation of pits. A more extensive study of the mechanism of pitting is currently in progress. Using a suitable barrier film between the ZrO_2 gate dielectric film and the Si electrode films can be one of the possible solutions for preventing this pitting in ZrO_2.

Our primary focus on the full flow transistor wafers was to test a variety of wet etches to remove the ZrO_2 remaining over the S/D areas. Figure 3 shows that pitting in the ZrO_2 film occurred on the full flow transistor wafers. Pitting was somewhat reduced by doing some optimization at the gate electrode etch process step. Very little pitting was observed after the ash step. Note that the 'rabbit ears' observed after the ash step are typically seen and they subsequently disappear after the resist cleans.

After gate etch | **After gate etch and ash** | **After gate etch, ash, and clean**

Figure 3 SEM image of pattered gate stack showing ZrO_2 over the source/drain areas

Various wet chemistries were tried to remove the ZrO_2 selectively over the S/D areas without etching the Si gate electrode, the Si substrate through the pits in the ZrO_2 films, or the STI field oxide. Wet etch using either HF, hot KOH or hot H_3PO_4 did not remove ZrO_2 effectively and resulted in significant damage to either Si or field oxide. RIE etch with CF_4 also resulted in substantial Si damage. Recently, we have successfully demonstrated a H_2SO_4 process that removed all ZrO_2 over the S/D areas and also did not result in any undercutting on the ZrO_2 underneath the gate electrode. It was also recently observed that HfO_2 behaves very differently compared to ZrO_2, and did not show any pitting under similar circumstances (see Figure 4). After the gate stack patterning, all the subsequent process steps were completed

without any issues. Functional transistors were successfully fabricated using ZrO_2 as well as HfO_2.

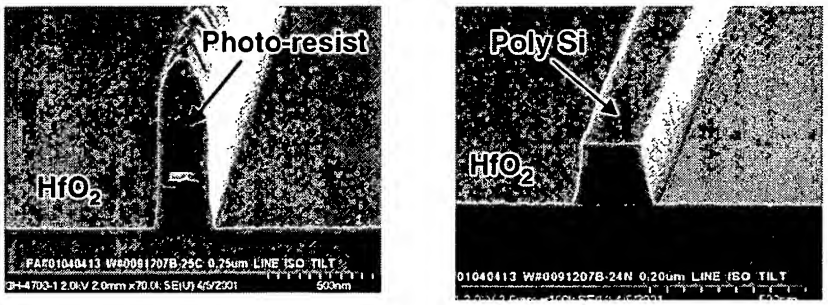

Figure 4 SEM image of patterned gate stack showing no signs of pitting in HfO_2 at all

REPLACEMENT GATE TRANSISTOR OPTION

Key high-k gate stack integration issues can be circumvented by using a replacement gate (RG) approach, also known as a 'damascence' gate transistor [21, 22]. This involves depositing the high-k gate dielectric film as well as the gate electrode after completing all the high temperature anneal steps. Thus, there is a significantly lower thermal stability requirement for the high-k gate stack. A number of high-k films that have been rejected due to their lower thermal stability limitations may now be viable candidates. Another major benefit of the RG approach is that the gate electrode etch stops on the pre-metal dielectric (PSG or BPSG). This eliminates many of the etch concerns like undercutting and substrate Si damage.

At ISMT, we have successfully fabricated RG transistors with ZrO_2 as the gate dielectric and Al/TaN as the gate electrode. Figure 5 shows the x-TEM of the transistor highlighting the well defined Al/TaN/ZrO_2/Si gate stack. Figure 6 illustrates several key transistor characteristics indicating good functional transistors.

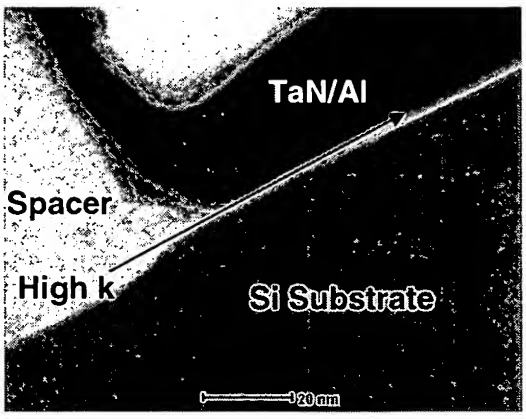

Figure 5 TEM of the edge of the replacement gate transistor gate stack with a ZrO_2 gate dielectric and an Al/TaN gate electrode

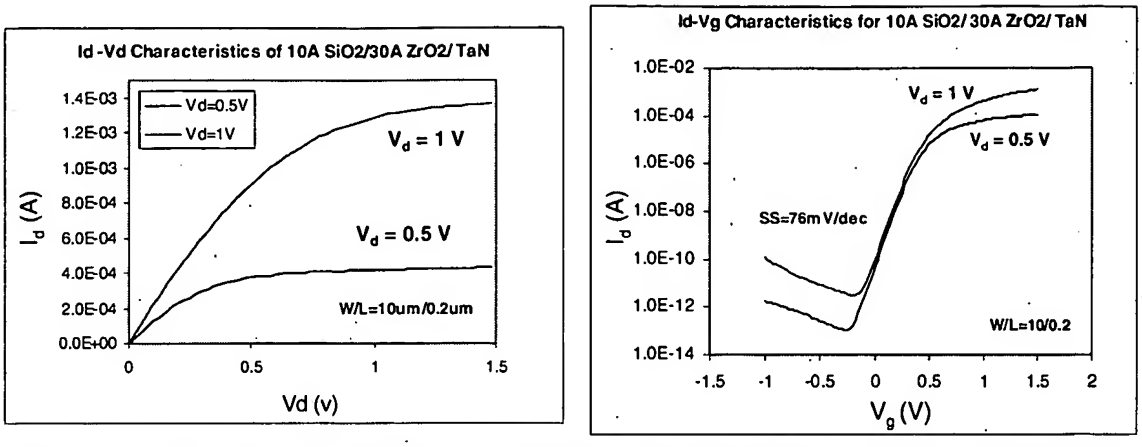

Figure 6 I_d-V_d and sub-threshold transistor characteristics of ZrO_2 replacement gate transistor fabricated at ISMT

Despite the benefits in integrating the high-k film with a metal electrode, the primary drawback associated with the RG is the higher cost associated with the additional process steps compared to the conventional transistor approach. Also, the RG transistor is a newer transistor structure and introduces many new process challenges such as removing the sacrificial (poly-Si on SiO_2) gate selectively without damaging either the Si substrate or the pre-metal dielectric. It also remains to be seen if the RG transistor can be scaled down to as low as 30 nm gate length that has been demonstrated on the conventional transistor.

SUMMARY

There are serious process challenges to integrating the high-k gate dielectric films to the conventional CMOS process flow. It is very important to start focusing on these issues as early as possible despite the fact that there in no consensus yet on the final choice. At ISMT, we have addressed many of the contamination issues related to introducing high-k materials to a production fab by developing a wafer backside clean and also by setting up many new fab protocols for handling the wafers with high-k films. Some of the wet and dry etch challenges in defining the high-k gate stack were addressed by using a variety of dry and wet etch processes. The thermal stability of the high-k films and its interaction with the Si substrate and electrode is very critical and it is likely that barrier layer films may be required. It is also likely that new annealing technologies may be needed. We were successful in fabricating functional conventional transistors using both ZrO_2 and HfO_2 gate dielectric films with poly-Si electrodes, although electrical performance was affected by the lower temperature S/D thermal activation processes used in this initial attempt. The replacement gate transistor helps address some of the high-k gate stack integration issues. However, additional processing steps are likely to add to the processed wafer cost. Also, substantial additional development is needed on the replacement gate transistor to demonstrate the same level of performance and scalability compared to the conventional transistor structure.

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